3D stacked (foveros) SOC power delivery analysis methodology for predictable silicon success.

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Agenda

- Introduction to Foveros.
- Foveros PDN challenges and opportunity.
- Foveros PDN analysis methodology.
- Foveros PDN simulation Results.
- Summary and Conclusion.

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Motivation

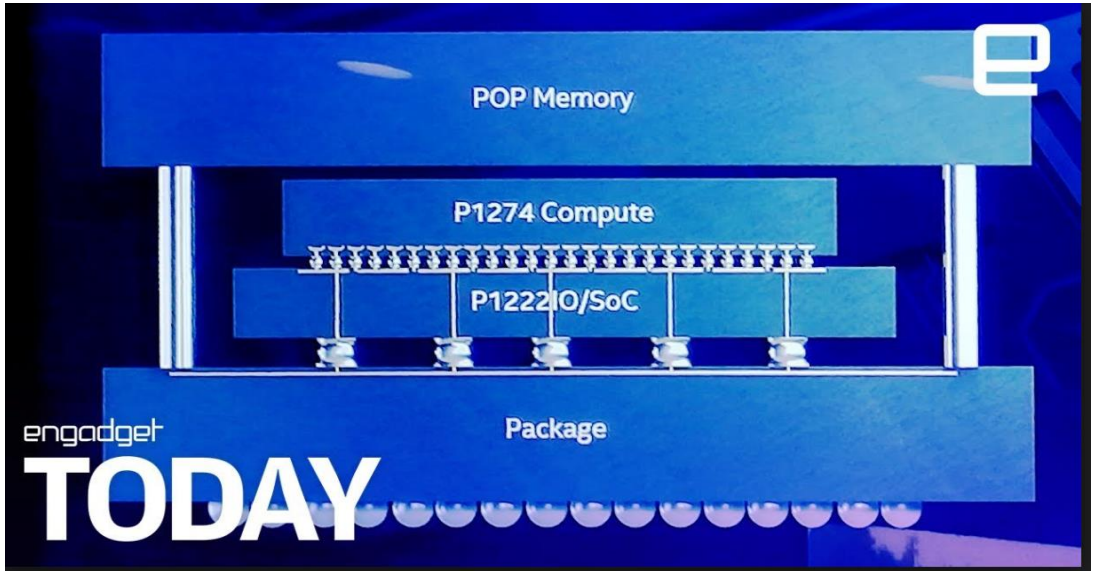


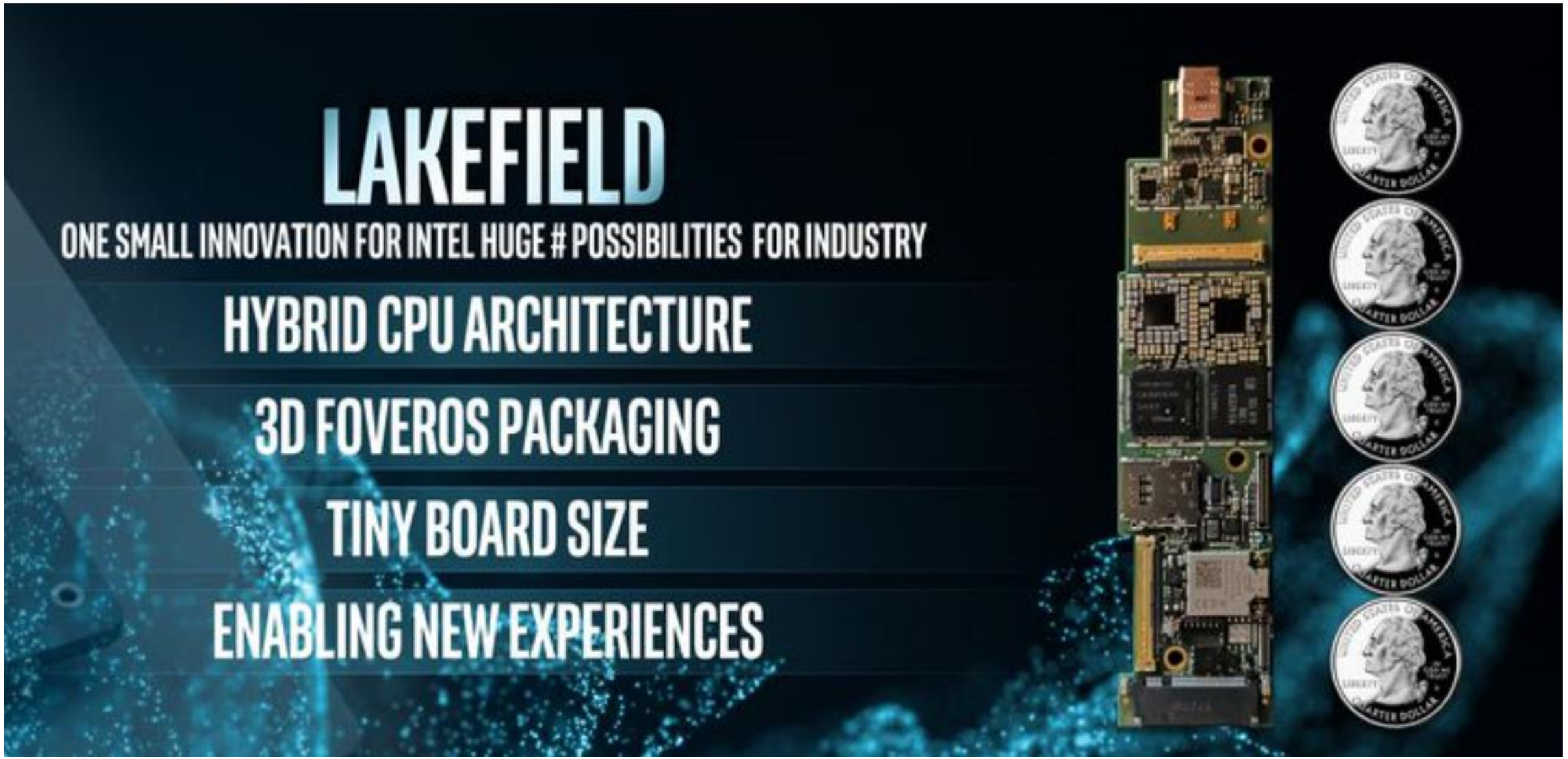
Diagram source: Intel Architecture Day 2019 Press release

Intel Foveros technology is to stack computing circuits on top of each other and wire them together with speedy connections, enabling it to pack more onto a single chip. Stacking has been used in memory chips before, but Intel would be the first company to successfully stack the so-called “logic” chips that handle computing tasks. When multiple die stacks with through silicon via ,Top die power delivery is through bottom die stack. This poses immense challenge due to shared voltage rails and common ground across Dies. The motivation is to share the methodology to analyze power delivery network of stacked die SOC, where power for compute pass through base die , having common shared rails between two dies and having common ground .

Power Integrity challenges require robust concurrent signoff methodology

-Figure out weak connections in context of die to die stacking using concurrent use cases .

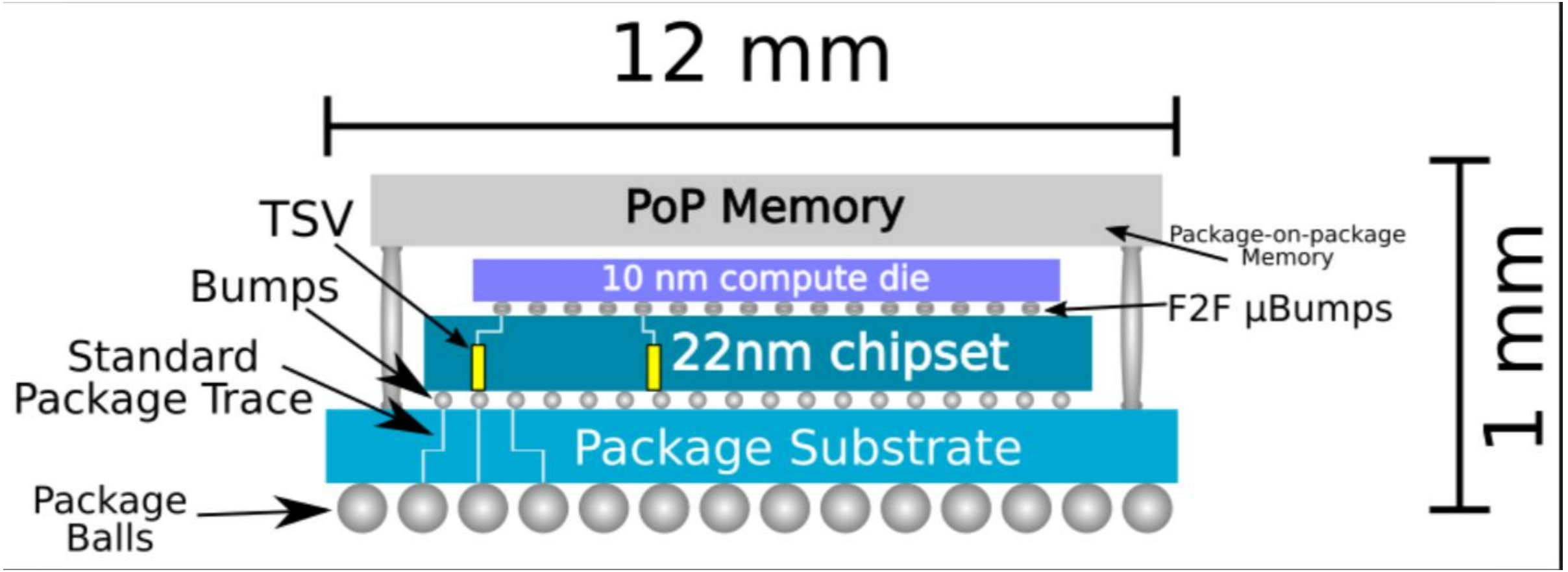
-Accurate voltage on top die in context of bottom die power demand



An entire computer board that’s no bigger than **five quarters laid end to end**

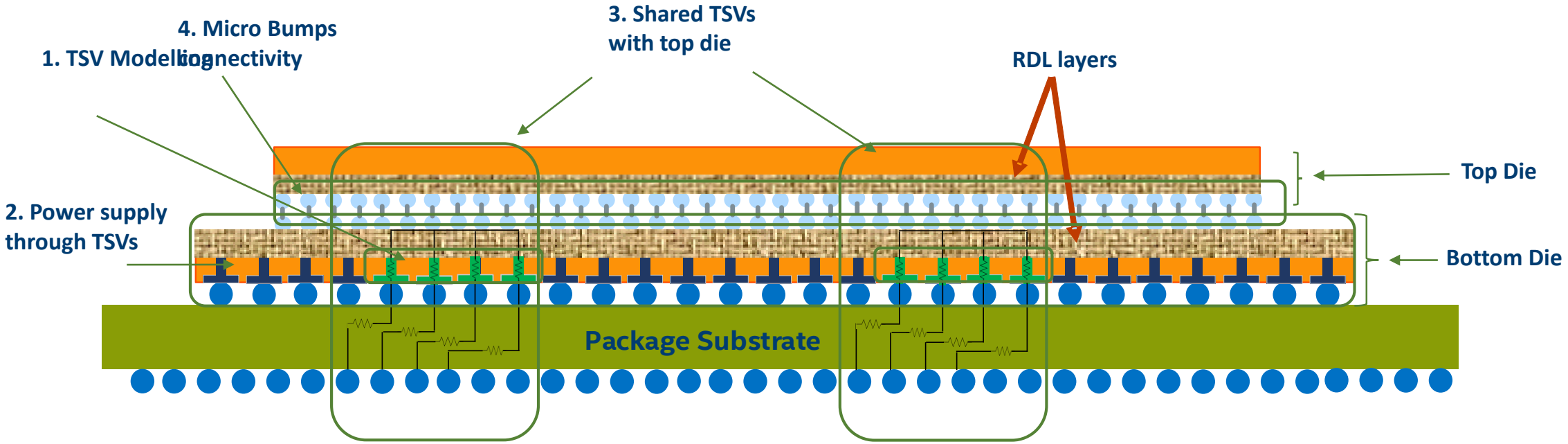
Sources : CES press conference

Foveros: The 3D stacking technology



Source : Intel Architecture Day 2019 Press release

Foveros PDN challenges



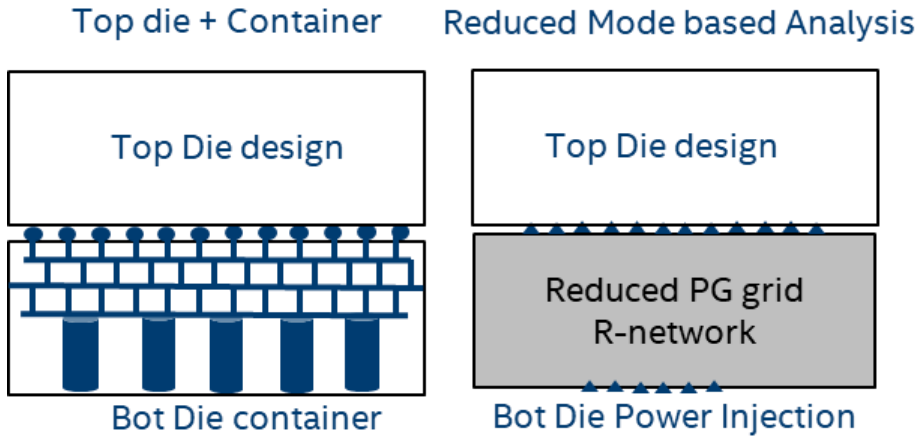
- ❑ Modeling of Through Silicon Via (TSV)
- ❑ Top die power delivery through bottom die
- ❑ Shared power rails and common ground across dies

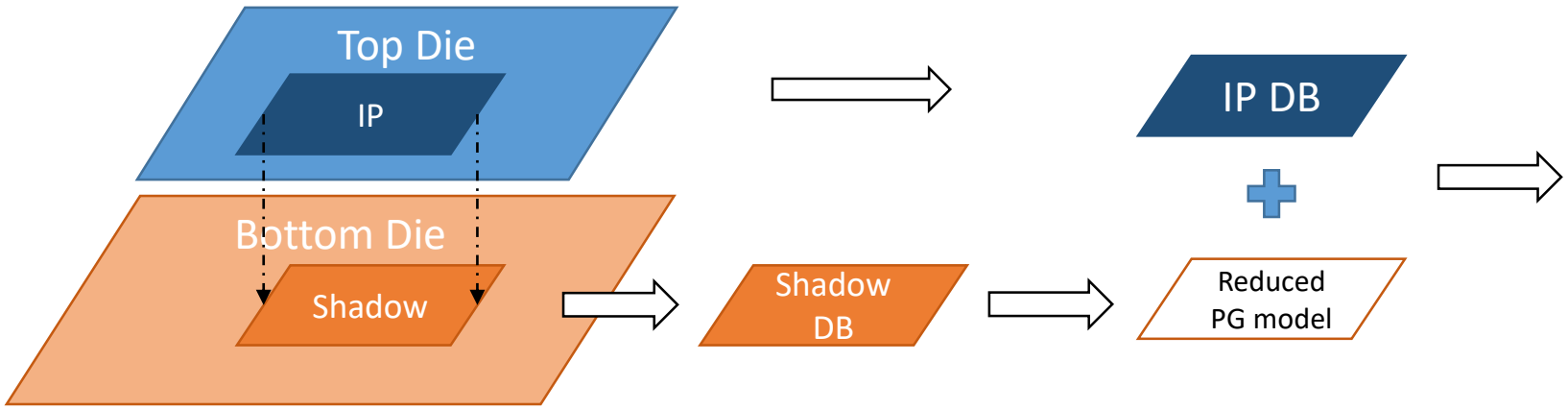
- ❑ Die to die micro-bump connectivity
- ❑ Limitation of implementation tools
  - Foveros is used first time in the industry for any production SOC, no vendor tool is available with proven silicon record

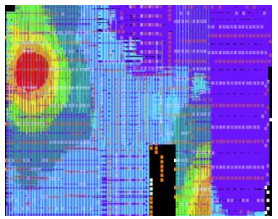
Power Integrity Methodology

Early analysis for Design convergence

- Bottom Die Containers created by cookie cut on shadow regions of Critical Top die IPs.
- PG network in container DB is modeled as reduced mxn multi-port R network
- Critical IP standalone runs included container reduced models to account for bottom die impact & voltage droop





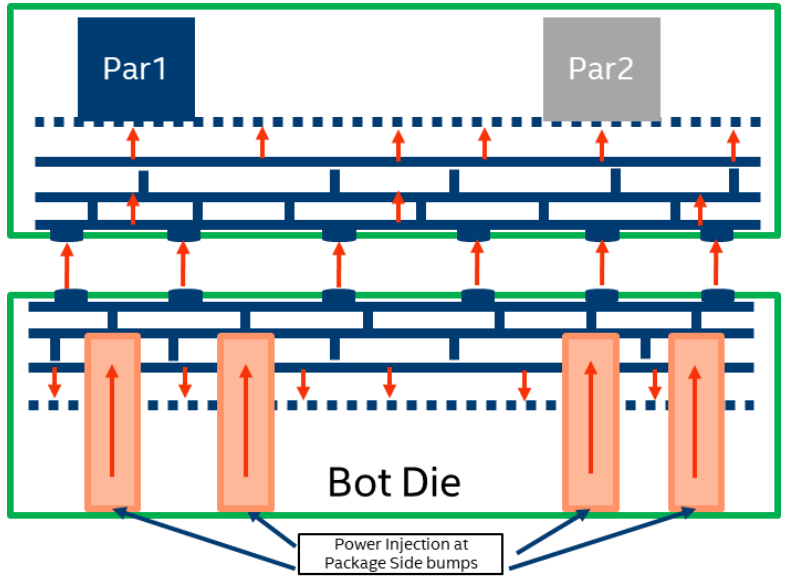


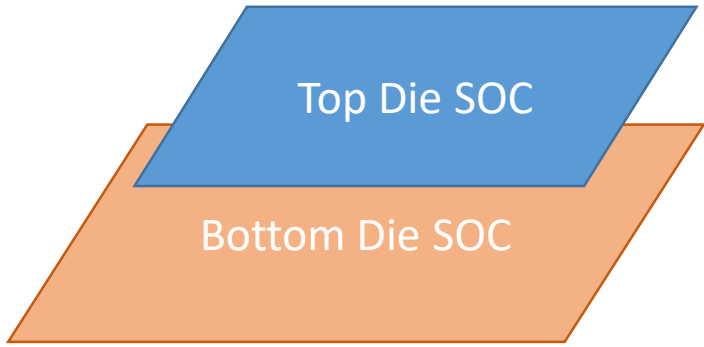
IR Drop Analysis of Top Die IP including bottom die reduced PG model

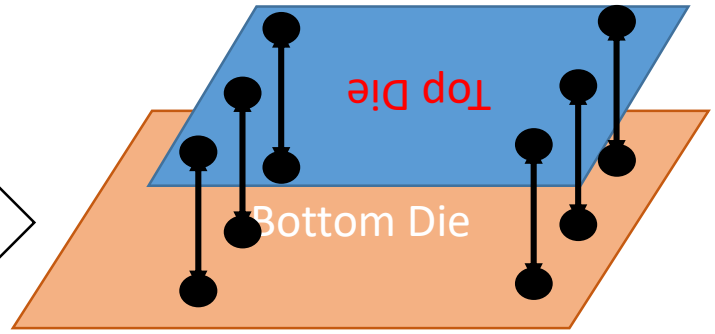
Power Integrity Methodology

Concurrent dual-die analysis for power delivery check

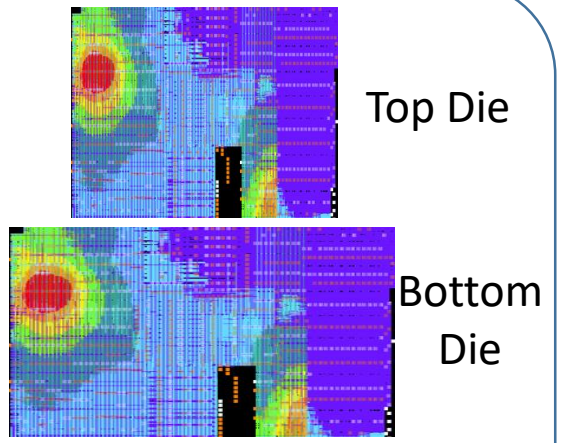
- Individual Die runs to ensure intra-die robust connectivity from micro Bump to logic
- Concurrent 3D-IC voltage droop analysis with both die stitched together







Offset & Orientation adjustments for bump mapping



Concurrent 3D-IC IRdrop Analysis

Design Convergence Process

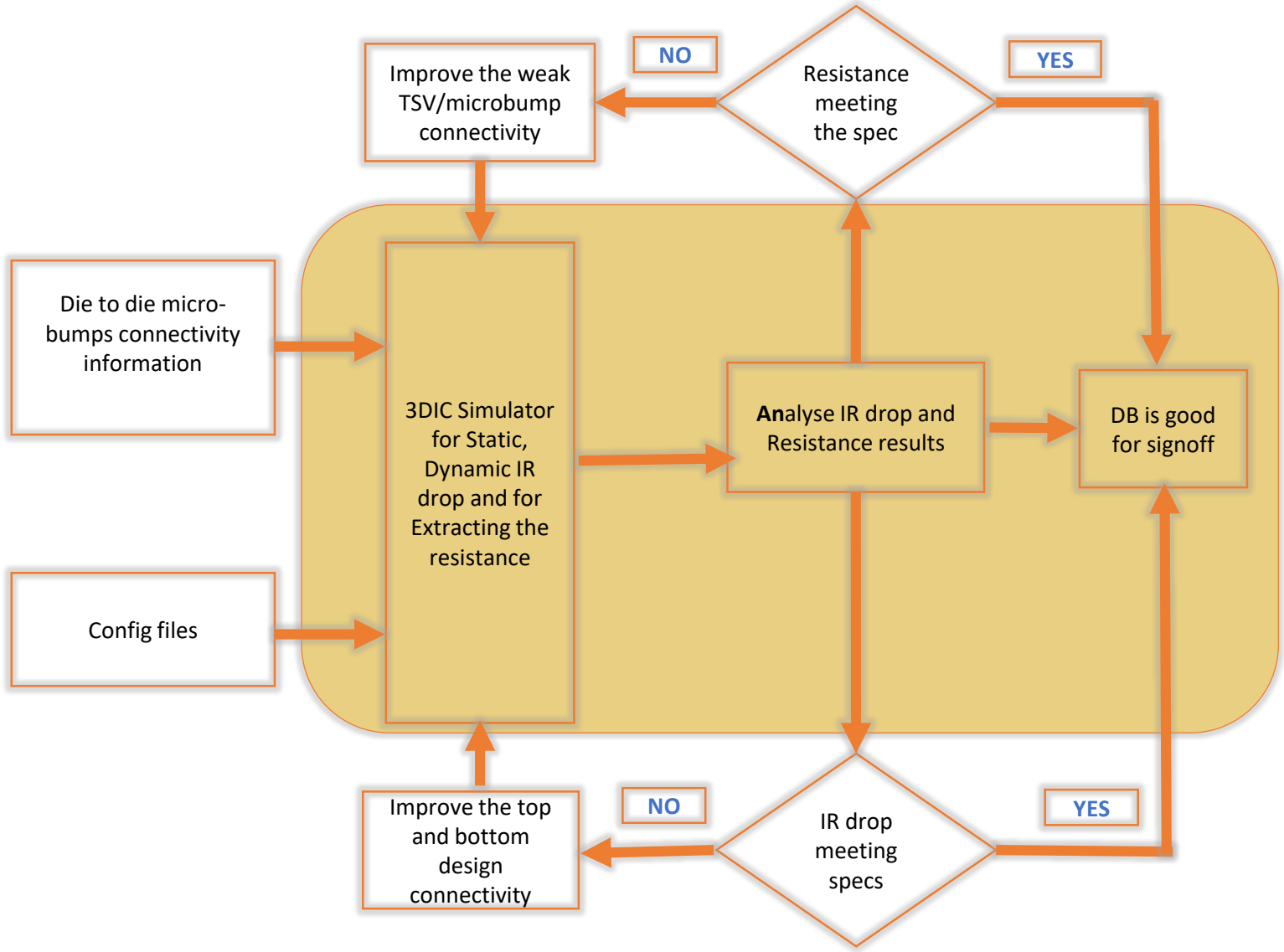
Vendor EDA tool with 3D-IC support enabled dual die concurrent analysis

- Bottom and Top die SOC fullchip database on different process nodes stitched together with appropriate tech collaterals
- X-die path tracing of IRdrop rootcause analysis on problematic areas
- Visual representation of hotspots in concurrent GUI

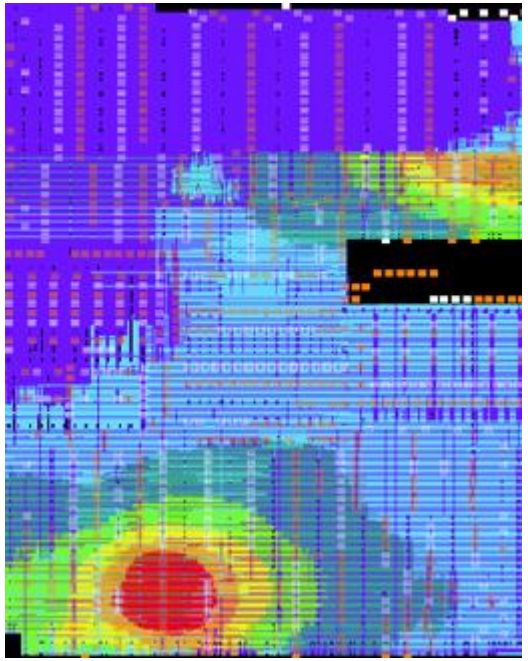
Signoff strategy

- Early runs to clean up gross issues at fullchip database - Runs used fullchip database without including sub hierarchies to find out RDL route and bump connectivity related issues. Power assignment done on sub hierarchy pins to account for power demands.
- Selectively opened up the critical power hungry sub-hierarchies – Runs added sub hierarchy DBs. Special attention on gated power rails tracing to ensure robust connectivity and adequate count of switch cells
- Signoff runs by opening up all sub-hierarchies from both the dies.

3D-IC Sign-off Strategy – Flow Diagram



Results



Red Area are hot spots and fixed using layout optimizations

- 3DIC PDN analysis flow and methodology developed.
- Two dies PDN network extracted in SOC context .
- The methodology is used for optimizing the TSV and PG grid .

3D IC based power delivery analysis helped to identify weaker spots

Summary & Conclusion

- Concurrent analysis is a must for multi die stacking technology sharing voltage rails and common ground
- The described methodology helped to find out multiple design issues related to die to die connectivity weakness.
- It also helped optimizing the TSV count and PG grid .
- Separate strategy for early and signoff analysis helped the design to converge faster.

Conclusion : Power delivery analysis methodology is developed to analyze staked die SOC design, to find weaker spots and addressed before tape-out to ensure design meets the target power delivery network impedance and meets power supply noise requirements .

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Q & A